

TYPES SN5480, SN7480 GATED FULL ADDERS

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logic

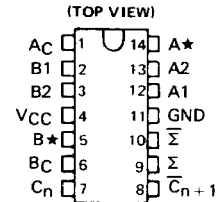
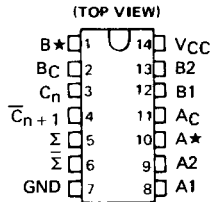
SN5480 . . . J PACKAGE
SN7480 . . . J OR N PACKAGE

SN5480 . . . W PACKAGE

FUNCTION TABLE
(See Notes 1, 2, and 3)

| INPUTS | | | OUTPUTS | | |
|--------|---|---|-----------------|----------|----------------|
| C_n | B | A | \bar{C}_{n+1} | Σ | $\bar{\Sigma}$ |
| L | L | L | H | H | L |
| L | L | H | H | L | H |
| L | H | L | H | L | H |
| L | H | H | L | H | L |
| H | L | L | H | L | H |
| H | L | H | L | H | L |
| H | H | L | L | H | L |
| H | H | H | L | L | H |

H = high level, L = low level



- NOTES: 1. $A = \bar{A}_C + \bar{A}^* + A1 \cdot A2$, $B = \bar{B}_C + \bar{B}^* + B1 \cdot B2$.
 2. When A* is used as an input, A1 or A2 must be low. When B* is used as an input, B1 or B2 must be low.
 3. When A1 and A2 or B1 and B2 are used as inputs, A* or B*, respectively, must be open or used to perform dot-AND logic.

description

These single-bit, high-speed, binary full adders with gated complementary inputs, complementary sum (Σ and $\bar{\Sigma}$) outputs and inverted carry output are designed for medium-and high-speed, multiple-bit, parallel-add/serial-carry application. These circuits (see schematic) utilize diode-transistor logic (DTL) for the gated inputs, and high-speed, high-fan-out transistor-transistor logic (TTL) for the sum and carry outputs and are entirely compatible with the TTL logic families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|---|----------------|
| Supply voltage, V_{CC} (see Note 4) | 7 V |
| Input voltage (see Note 5) | 5.5 V |
| Operating free-air temperature range: SN5480 Circuits | -55°C to 125°C |
| SN7480 Circuits | 0° to 70°C |
| Storage temperature range | -65°C to 150°C |

- NOTES: 4. Voltage values are with respect to network ground terminal.
 5. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions

| | SN5480 | | | SN7480 | | | UNIT |
|---------------------------------------|----------------------------|-----|------|--------|-----|------|---------|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, V_{CC} | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level output current, I_{OH} | Σ or $\bar{\Sigma}$ | | -400 | | | -400 | μ A |
| | \bar{C}_{n+1} | | -200 | | | -200 | |
| | A* or B* | | -120 | | | -120 | |
| Low-level output current, I_{OL} | Σ or $\bar{\Sigma}$ | | 16 | | | 16 | mA |
| | \bar{C}_{n+1} | | 8 | | | 8 | |
| | A* or B* | | 4.8 | | | 4.8 | |
| Operating free-air temperature, T_A | -55 | | 125 | 0 | | 70 | °C |

PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

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TYPES SN5480, SN7480 GATED FULL ADDERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | SN5480 | | | SN7480 | | | UNIT |
|-----------------|--|--|--|--------|------|-----|--------|------|-----|------|
| | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| V _{IH} | High-level input voltage | | | 2 | | | 2 | | | V |
| V _{IL} | Low-level input voltage | | | 0.8 | | | 0.8 | | | V |
| V _{OH} | High-level output voltage | Σ or Σ | V _{CC} = MIN, I _{OH} = -400 μA | 2.4 | 3.5 | | 2.4 | 3.5 | V | |
| | | C _{n+1} | V _{IH} = 2 V, I _{OH} = -200 μA | | | | | | | |
| V _{OL} | Low-level output voltage | A* or B* | V _{IL} = 0.8 V, I _{OH} = -120 μA | 0.22 | 0.4 | | 0.22 | 0.4 | V | |
| | | Σ or Σ | V _{CC} = MIN, I _{OL} = 16 mA | | | | | | | |
| V _{OL} | Low-level output voltage | C _{n+1} | V _{IH} = 2 V, I _{OL} = 8 mA | 0.22 | 0.4 | | 0.22 | 0.4 | V | |
| | | A* or B* | V _{IL} = 0.8 V, I _{OL} = 4.8 mA | | | | | | | |
| I _I | Input current at maximum input voltage | V _{CC} = MAX, V _I = 5.5 V | | 1 | | | 1 | | | mA |
| I _{IH} | High-level input current | A ₁ , A ₂ , B ₁ , B ₂ , A _C , or B _C | V _{CC} = MAX, V _I = 2.4 V | 15 | | | 15 | | | μA |
| | | A* or B* | | -1.1 | | | -1.1 | | | |
| | | C _n | | 200 | | | 200 | | | |
| I _{IL} | Low-level input current | A ₁ , A ₂ , B ₁ , B ₂ , A _C , or B _C | V _{CC} = MAX, V _I = 0.4 V | -1.6 | | | -1.6 | | | mA |
| | | A* or B* | | -2.6 | | | -2.6 | | | |
| | | C _n | | -8 | | | -8 | | | |
| I _{OS} | Short-circuit output-current‡ | Σ or Σ | V _{CC} = MAX | -20 | | | -18 | | | mA |
| | | C _{n+1} | | -20 | | | -18 | | | |
| | | A* or B* | | -0.9 | | | -2.9 | | | |
| I _{CC} | Supply current | V _{CC} = MAX, See Note 6 | | 21 31 | | | 21 35 | | | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

NOTE 6: I_{CC} is measured with all inputs and outputs open.

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switching characteristics, V_{CC} = 5 V, T_A = 25°C

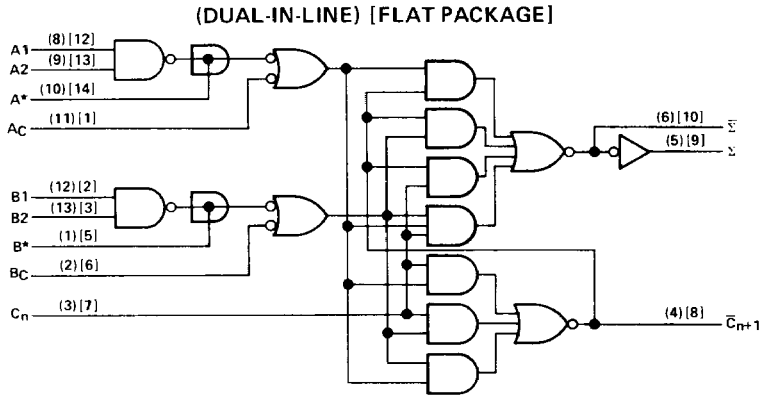
| PARAMETER¶ | FROM INPUT | TO OUTPUT | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|----------------|------------------|--|-----|-----|-----|------|
| t _{PLH} | C _n | C _{n+1} | C _L = 15 pF, R _L = 780 Ω, See Note 7 | 13 | 17 | ns | |
| t _{PHL} | | | | 8 | 12 | | |
| t _{PLH} | B _C | C _{n+1} | | 18 | 25 | | |
| t _{PHL} | | | | 38 | 55 | | |
| t _{PLH} | A _C | Σ | | 52 | 70 | | ns |
| t _{PHL} | | | | 62 | 80 | | |
| t _{PLH} | B _C | Σ | 38 | 55 | | | |
| t _{PHL} | | | 56 | 75 | | | |
| t _{PLH} | A ₁ | A* | C _L = 15 pF, See Note 7 | 48 | 65 | ns | |
| t _{PHL} | | | | 17 | 25 | | |
| t _{PLH} | B ₁ | B* | | 48 | 65 | | |
| t _{PHL} | | | | 17 | 25 | | |

¶ t_{PLH} = propagation delay time, low-to-high-level output

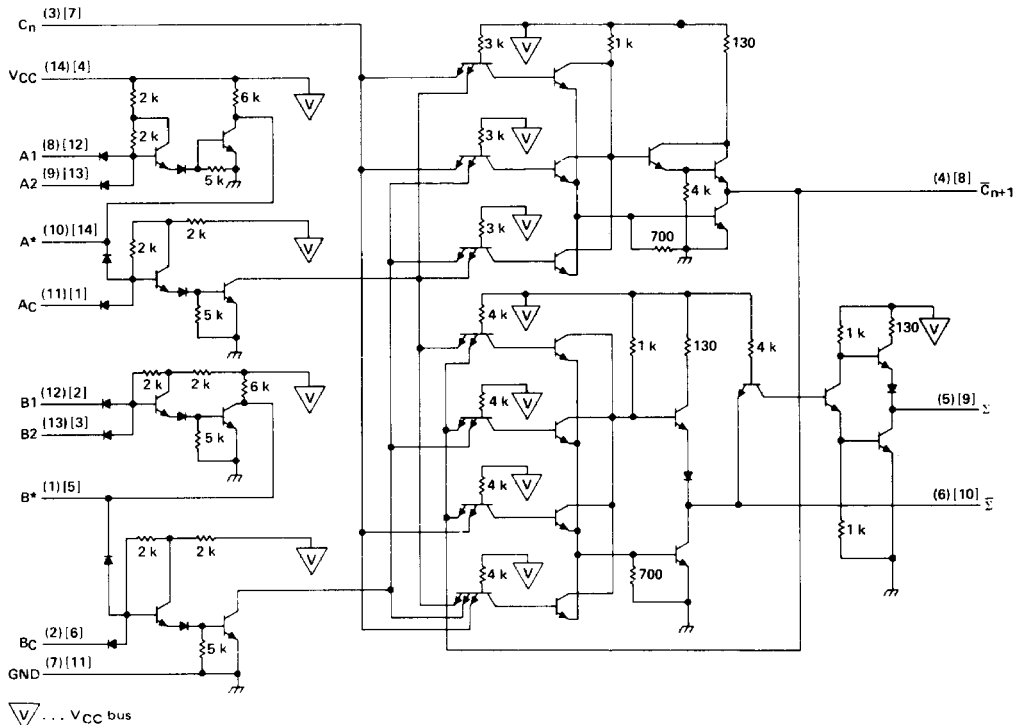
t_{PHL} = propagation delay time, high-to-low-level output

NOTE 7: The load for testing outputs A* and B* consists only of capacitance C_L to ground. See General Information Section for load circuits and voltage waveforms.

logic diagram



schematic



Resistor values shown are nominal and in ohms.
Pin numbers shown in () are for the N or J package and pin numbers shown in [] are for the W package.

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